Please cancel claim 20.

REMARKS

Amendment to the Specification

The Specification has been amended to incorporate subject matter present in claim 1 as originally filed. Accordingly, it is believed that the amendment presents no new matter.

Rejections Under 35 U.S.C. §112, Second Paragraph

Claim 1 has been amended to overcome the first ground for this rejection.

While it is believed that the term etch stop was described, and would be understood by one skilled in the art[1], the Specification has been amended to further clarify the term.[2] It is noted that particular contact hole etches are also described in the Specification.[3]

Rejection of Claim 1 Under 35 U.S.C. §103(a), *Sakai et al.* (5,503,901) in view of *Chang et al.*(5,893,740).

The invention of claim 1 includes a method of forming a contact hole that is self-aligned with a transistor gate having a gate length of less than 0.2 μm. Further, the contact hole can be formed without an etch stop liner for a contact hole etch. This is in contrast to conventional approaches that include an etch stop liner.

While larger scale devices (i.e., devices with transistor gate lengths substantially greater than 0.2 μm) have had various approaches to forming contact holes, as noted in

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[1] From 1996 to the present, the USPTO issued 2365 patents containing the phrase "etch stop" (see attached printout), 610 of which include "etch" and "stop" in the claims.
[2] See the Specification, Page 4, Line 22 which first refers to an etch stop. The amendment further clarifies that a liner layer can be an etch stop for a contact hole etch.
[3] See the Specification, Page 8, Line 10, Page 13, Lines 6-14, Page 16, Lines 16-17.

the Specification, conventional approaches to contacts of 0.2 μm and less, have included etch stop layers to avoid unwanted etch results.[4] It is believed that the invention of claim 1 transcends the prior art by reciting a method that not only (1) forms a contact hole that is self-aligned with a transistor gate, where (2) having a gate length of less than 0.2 μm, and (3) does so without forming an etch stop liner. It is not believed that any combination of the cited references, *Sakai et al.* in view of *Chang et al.*, can suggest such an approach.

Firstly, *Sakai et al.* and *Chang et al.* present technologies having considerable differences. For this reason, it is believed that it would not be obvious to combine the references. Secondly, both are silent with respect to key elements of the other reference, thereby failing to suggest the desirability or reasonable potential for success of the combination.

Sakai et al. is directed toward an etch that is selective between silicon oxide and silicon nitride.[5] As noted in the Office Action, *Sakai et al.* does not teach a method that forms a contact hole self-aligned with a transistor gate having a length of less than 0.2 μm. Thus, *Sakai et al.* shows a conventional etch for a larger scale device. While *Chang et al.* shows the formation of a transistor having a gate length that is typically 0.1 μm or less, it is noted that the transistor is a short channel transistor having specific structures and requirements for proper operation. More particularly, as noted in *Chang et al.*, short channel transistors may include many serious problems.[6] It is believed that these particulars argue against combination.

It is further noted that *Sakai et al.* is entirely silent with respect to the formation a structure having a gate length of less than 0.2 μm. Therefore, it is not believed that the reference provides any indication that the described etch would work for gate lengths less than 0.2 μm without an etch stop. At the same time, *Chang et al.* is completely silent

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[4] See the Specification, Page 5, Line 24. See also Page 8, Lines 17-20 for general protective properties of an etch stop (i.e., a liner).

[5] See *Sakai et al.*, Col. 1, Lines 6-10 discussing the Technology of the Invention.

[6] See *Chang et al.*, Col. 1, Lines 10-19 describing the presence of short channel effects generally, and the serious problem of punchthrough in particular.

with respect to the formation contacts. Thus, it is not believed that *Chang et al.* provides indication that a self-aligned contact without an etch stop would work for structure having gate lengths of less than 0.2 μm.

Accordingly, because the invention of claim 1 includes limitations not present in, or suggested by the cited combination of references, it is believed that the rejection of claim 1 is traversed.

Rejection of Claims 2-11 Under 35 U.S.C. §103(a), *Sakai et al.* (5,503,901) in view of *Chang et al.*(5,893,740), and further in view of *Nulty et al.* (5,468,342).

To the extent that this rejection relies on the combination of *Sakai et al* in view of *Chang et al.*, the arguments set forth for claim 1 are incorporated by reference herein.

It is initially noted that *Nulty et al.* presents a conventional approach that includes an etch stop liner.[7] Therefore, at best, *Nulty et al.* fails to distinguish between approaches that include etch stop liners and those that do not include etch stop liners. Because *Nulty et al.*, only shows examples of methods that include an etch stop liner, it is not believed that it would have been obvious combine the teachings of *Nulty et al.* with the other cited references and arrive at a method that does not include an etch stop liner.

With respect to claim 3 in particular, the invention of claim 3 depends form claim 1, and further includes reactive plasma etching through an insulating layer comprising doped silicon dioxide, where a phosphorous doping concentration is greater than 5% by weight. Because the cited references are silent as to this particular level of doping concentration, it is believed that this rejection is unsustainable.

Sakai et al. indicates that a silicon oxide film may include such impurities as boron, phosphorous, arsenic and so on.[8] However, *Sakai et al.* gives no indications as to concentration, let alone a high (with respect to conventional approaches) concentration of

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[7] See *Nulty et al.*, Fig. 4 and Col. 3, Lines 50-51, describing etch stop layer 403. See also, Figs. 12-14 and Col. 10, Lines 42-49, which discuss etch stop layer 1203, and Figs. 15-17, which show an etch stop layer 1503.

[8] See *Sakai et al.*, Col. 5, Lines 40-42.

phosphorous set forth in claim 3. *Chang et al.* appears to be concerned only with the formation of the particular short channel transistor, and has no teachings regarding an insulating layer formed over such a device. *Nulty et al.* refers to oxide layers that may be doped with boron, phosphorous or both.[9] However, like *Sakai et al.*, particular concentrations are not discussed. As noted in the Specification, phosphorous concentrations over 5% can have undesirable effects. In light of this, and the fact that the cited references do not teach the claimed phosphorous dopant concentration, it is believed that claim 3 is patentable over the cited combination of references.

In light of all the above arguments, it is believed that the rejection of claims 2-11 is traversed.

Rejection of Claim 12 Under 35 U.S.C. §103(a), *Sakai et al.* (5,503,901) in view of *Nulty et al.* (5,468,342).

The invention of claim 12, as amended, includes etching a contact hole through a first insulating layer of doped silicon dioxide. Two etch selectivities are disclosed. A first selectivity is between the first insulating layer and the sidewall, and is greater than ten to one. A second selectivity is between the first insulating layer and the substrate, and is greater than one hundred to one. As noted in the Specification, by etching a first insulating layer with such selectivities between a sidewall and substrate, it may be possible to dispense with the need for a protective liner that is typically used in conventional approaches.[10]

Sakai et al. teaches etching with a selectivity between silicon oxide and silicon nitride of greater than twenty to one. However, *Sakai et al.* remains silent as to particular selectivities between an insulating layer and a substrate. *Nulty et al.*, like *Sakai et al.*, does not disclose the cited selectivity the insulating layer and the substrate, largely due to the presence of an etch stop layer between the insulating layer and substrate. Because

[9] See *Nulty et al.*, Col. 1, Lines 17-25.

both of the cited references are silent as to the claimed etch selectivity between the insulating layer and the substrate, it is believed that this rejection is traversed.

Rejection of Claims 13-17 Under 35 U.S.C. §103(a), *Sakai et al.* (5,503,901) in view of *Nulty et al.* (5,468,342).

To the extent that this rejection relies on *Sakai et al.*, the arguments set forth for claim 12 are incorporated by reference herein.

With respect to claim 14 in particular, the invention of claim 14 further includes forming a first insulating layer with a high density plasma and having a phosphorous dopant concentration that is greater than 5% by weight. It is believed that the plasma density and dopant concentration limitations are not present in, or suggested by the cited combination of references.

As noted in the discussion related to claim 3, while *Sakai et al.* and *Nulty et al.* refer to silicon oxide layers that may be doped with phosphorous, neither reference discloses or suggests the relatively high (with respect to conventional approaches) phosphorous dopant concentrations.

Still further, claim 14 recites a high density plasma. High density plasma charged particle density ranges are noted in the specification.[11] However, both *Sakai et al.* and *Nulty et al.* are silent as to the particulars of a plasma charge density involved in the formation of an insulating layer.

Because neither cited reference provides any teachings as to the formation of a silicon dioxide layer having a phosphorous doping concentration greater than 5%, nor a high density plasma for forming such a layer, it is believed that this rejection is traversed.

With respect claim 17 in particular, the invention of claim 17 includes a hard etch mask comprising silicon dioxide and a first insulating layer comprising phosphorous

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[10] See the Specification, Page 25, Lines 8-11 and Lines 18-20.
[11] See the Specification, Page 12, Lines 18-20.

doped silicon dioxide. Such an arrangement is not believed to be shown in, or suggested by the cited references.

Sakai et al. is silent as to hard etch masks. While *Nulty et al.* discloses particular types of hard masks[12], the materials disclosed are not suggestive of, and may actually teach away from a hard mask of silicon dioxide. Namely, after forming a hard mask, *Nulty et al.* describes an "oxide etch" for forming a contact hole. Such an oxide etch could substantially etch the hard mask itself. Thus, it is not believed that a hard etch mask of silicon oxide employed to etch an underlying layer of doped silicon oxide would be obvious. For these reasons, it is believed that the rejection of claim 17 is traversed.

Rejection of Claim 18 Under 35 U.S.C. §102(b), *Sakai et al.*

The invention of claim 18, as amended, includes a method of forming a hard mask of substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide. Such a hard mask may have openings at a contact hole location. A contact hole is formed at the contact hole location through the insulating layer. The contact hole is also formed between conducting structures separated from one another by less than 0.4 microns. It is believed that such an arrangement can be considered contrary to the approaches of the cited art, as a hard mask and underlying insulating material may both include silicon dioxide. The cited art does not appear to teach an etch that may distinguish between two layers that both include silicon dioxide.

As noted in the remarks related to claim 17, *Sakai et al.* is silent as to hard etch masks. Further, it not believed that the incorporation of a hard mask comprising undoped silicate glass to etch an underlying layer that also comprises silicon dioxide would be obvious. As noted above, absent the teachings of the present invention, it would be counter-intuitive to use an etch mask of silicon dioxide to etch an underlying layer that comprises silicon dioxide. Such an argument is supported by *Sakai et al.* itself. In fact, it is believed that *Sakai et al.* teaches away from claim 17.

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[12] See *Nulty et al.*, Col. 6, Lines 31-34, which indicate a hard mask may be formed from silicon nitride, aluminum, titanium silicide, tungsten, or other refractory metal.

Sakai et al. concentrates on achieving etch selectivity between silicon oxide and silicon nitride. As such, *Sakai et al.* appears to provides no difference in etch selectivity between oxide layers.[13] Without such a selectivity, there would be no motivation to form an etch mask according to claim 17.[14] Therefore, because *Sakai et al.* provides no motivation to arrive at the invention of claim 18, and may teach away from such claim limitations, it is believed that the rejection of claim 18 is traversed.

Claims 1-3 have been amended to overcome rejections based on 35 U.S.C. §112, second paragraph and to correct typographical errors, and not in response to the cited art. In addition, claims 12, 14 and 17 have also been amended. Claims 15 and 20 have been cancelled. The present claims 1-14 and 16-19 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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[13] See *Sakai et al.*, Col. 16, Lines 9-15, which indicates the invention can provide the given etching selectivity between silicon oxide and silicon nitride, but also between doped silicon oxide films, such as BPSG and ASSG (arsenic added silicate glass), and silicon nitride. This suggests similar etch rates for both doped and undoped silicon oxide.
[14] Various examples of the desirable etch selectivity between a hard mask and underlying insulating layer are described in the Specification at Page 25, Lines 13-17.